REMARKS

Claims 1-6 are currently pending in the above-identified patent application. In the subject Office Action, claim 2 was objected to because it was ended using a semi-colon. Applicants wish to thank the Examiner for having identified this clear typographical error, and have amended claim 2 by replacing the semi-colon with a period in accordance with the Examiner's suggestion. No new matter has been added by this change.

Claims 1-6 were rejected under 35 U.S.C.102(b) as being anticipated by Miller et al. (U.S. Patent No. 6,539,531), since the Examiner stated that as to claims 1, and 4 Miller et al. teaches a method of analyzing the effects of a high-frequency transmission system comprising: modeling a high-frequency signal source as an ideal voltage source and a resistance and capacitance circuit (Fig. 16; Fig. 19; Col. 3, line 52 to Col. 4, line 9; Col. 13, line 21 to Col. 18, line 58, especially Col. 17, line 40 to Col. 18, line 28 of Miller et al.); modeling bond wire connections within said transmission system using an equivalent resistance, capacitance and inductance circuit (Col. 13, lines 22-35 of Miller et al.); modeling an integrated-circuit package in said transmission system using an equivalent resistance, capacitance and inductance circuit (Col. 4, line 10 to Col. 5, line 35 of Miller et al.); modeling a package stub in said transmission system as an unterminated transmission line (Col. 4, line 10 to Col. 5, line 35; and Col. 13, lines 22-35 of Miller et al.); and selecting a package trace such that the length of said package stub is sufficiently short so that transmission line effects of said package stub occur at a frequency higher than the highest-expected frequency used by said package trace (Fig. 16; Fig. 19; Col. 3 line 52 to Col. 5, line 9; and Col. 13, line 21 to Col. 18, line 58, and especially Col. 17, line 40 to Col. 18, line 28 of Miller et al.).

As to claims 2, and 5, the Examiner continued that Miller et al. teaches modeling a trace wire of a printed circuit board in said transmission system using an equivalent resistance, capacitance and inductance circuit (Col, 13, lines 22-35 of Miller et al.); and as to claims 3, and 6, Miller et al. teaches modeling a printed circuit board stub as an unterminated transmission line (Col. 13, lines 22-35 of Miller et al.), and selecting a printed circuit board trace such that the length of said printed

circuit board stub is sufficiently short so that the transmission line effects of said package stub occur at a frequency higher than the highest expected frequency of a signal applied to said trace wire (Fig. 16; Fig. 19; Col. 3 line 52 to Col. 5 line 9; and Col. 13, line 21 to Col. 18, line 58, and especially Col. 17, line 40 to Col. 18, line 28 of Miller et al.).

Applicants respectfully disagree with the Examiner concerning this ground of rejection for the reasons to be set forth herein below.

Page 3, lines 9-30 of the present Specification, as originally filed, provide definitions of package trace and package stub: "Figure 1 illustrates the top view of a typical integrated-circuit (IC) package 102 and an integrated circuit (IC) chip 104 mounted on IC package 102. The chip 104 has a series of bond pads 106 that provide an electrical connection to the chip 104. Bond wires 108 are connected to bond pads 106 on the chip 104. Bond wires 108 connect to a ring of bond posts 110 on the integrated-circuit package 102. The bond posts 110 of the IC package 102 are connected to package traces 112. The package traces 112 are disposed in various layers of the IC package 102 and provide connections to solder balls, such as solder ball 114, that are disposed on the bottom of the IC package 102. In addition, the package signal traces 112 extend to the package edge 120 from the solder balls, such as solder balls 114, 116. The portion of the package trace 112 that extends from the solder balls to the package edge 120 is referred to as the stub. For example, stub 122 extends from the solder ball 114 to the package edge 120. Similarly, stub 124 extends from the solder ball 116 to package edge 120. The stubs provide a method, during manufacturing of the IC package 102, to insure that there is proper conductivity of the package traces 112. So, for example, during manufacture and testing of the IC package 102, a test device is connected to the stub at the package edge 120 to test conductivity between the stub and the bond post. More specifically, one lead of an ohm meter may be connected to stub 122 at the package edge 120 and the other lead of the ohm meter can be connected to bond post 118, to determine if there is proper conductivity. Each of the package traces 112 is tested in this manner during the manufacture of the IC package 102.

Hence, the stubs, such as stubs 122, 124, merely function as a connector to test the package traces 112 and are left unterminated at the package edge 120."

Page 9, line 4 to page 10, line 2 of the present Specification, as originally filed, sets forth the procedure for determining desired stub length as follows: "Hence, the three package traces 702, 710 and 716 disclosed in Figure 7 illustrate the fact that, in general, as the length of the package trace between the bond post and the solder ball increases, the length of the stub shortens. Since it is normally desirable to have a short trace length between the bond post and the solder ball, it is counterintuitive to select a package trace, such as package trace 716, which has a long length between bond post 726 and solder ball 718 for higher frequency signals, since the equivalent RLC circuit will have a greater impedance between the bond post 726 and solder ball 718, than a package trace such as package trace 702 which has a lower equivalent circuit impedance between bond post 722 and solder ball 704. However, the short length of package trace 702, between bond post 722 and solder ball 704, creates a long stub 706. If a low frequency signal is applied to package trace 702, the length of the stub 706 is likely to be irrelevant. However, if the signal path 702 is used for high frequency signals, and the quarter wavelength is an odd integer multiple of the length of the stub 706, transmission line effects will occur and the attenuation created by stub 706 as a result of transmission line effects may severely attenuate such a high frequency signal.

In other words, high frequency signals should employ package trace 716, which has the shortest stub 720 of the three signal paths in Figure 7. Stub 720 will cause transmission line effects at the highest frequency of the three package traces 702, 710 and 716. By treating the stubs 706, 714 and 720 as unterminated transmission lines and selecting signal traces in accordance with the frequency of the signals traveling on the package traces 702, 710 and 716, signals can be transmitted in the package without creating unexpected transmission line effects and severe attenuation. Similar techniques of analyzing the PC board stub 439, in the integrated circuit and any other stubs that exist in the IC system and integrated circuit can be used to insure that severe attenuation does not occur as a result of transmission line effects.

The present invention therefore provides a method for analyzing a high frequency transmission system to avoid transmission line effects. By selecting a trace with a short stub length, the frequency at which transmission line effects appear is higher. If the highest signal frequency applied to that trace is lower than the frequency at which transmission line effects occur, transmission line effects will be prevented."

Turning now to the Examiner's rejection of subject claims 1 and 4 as being anticipated by Miller et al. and, in particular, to the following language of claim 1: "... selecting a package trace such that the length of said package stub is sufficiently short so that transmission line effects of said package stub occur at a frequency higher than the highest-expected frequency used by said package trace.", the Examiner stated that Fig. 16; Fig. 19; Col. 3 line 52 to Col. 5, line 9; and Col. 13, line 21 to Col. 18, line 58, and especially Col. 17, line 40 to Col. 18, line 28 of Miller et al. anticipates this recitation. Applicants respectfully disagree with the Examiner concerning this conclusion. For example, Col. 5, lines 2-9 state: "As I/O signal frequencies increase, the design of structures we use to link a wafer-level IC tester to test points on an IC wafer becomes increasingly problematic. When wafer-level IC tester interconnect systems do not have the same frequency response characteristics as interconnect systems employed in an IC's intended operating environment, then many ICs that would operate properly in their intended operating environment can fail tests and be rejected or de-rated." Subject claims 1 and 4 relate to a package stub which is part of an IC package, while the passage quoted by the Examiner from Miller et al. describes a wafer-level tester.

Column 3, line 52 to Col. 4, line 8 states: "In high frequency applications an interconnect system can severely attenuate and distort signals passing between the IC and external circuits. The conventional approach to reducing the amount of signal distortion and attenuation caused by the interconnect system has been to minimize the series inductance and shunt capacitance of the interconnect system. Much of the inductance in packaged IC interconnect system comes from bond wires and package legs or spring contact. Designers try to minimize that inductance by keeping the bond wires and package legs or spring contacts as short as possible.

Interconnect system capacitance arises mainly from the capacitances of bond pads and printed circuit board (PCB) traces, and the capacitances of terminating devices within the IC such as drivers, receivers and electrostatic discharge protection (ESD device) devices. Designer try to minimize the interconnect system capacitance when designing such components. However, while minimizing interconnect system inductance and capacitances can help improve bandwidth, flatten frequency response and reduce signal distortion, it is not possible to completely eliminate interconnect system inductance and capacitance. Thus, some level of signal distortion and attenuation in an interconnect system is inevitable, and can become problematic particularly at high signal frequencies." Subject claims 1 and 4, by contrast, recite the proper selection of package traces such that the package stub does not generate transmission line effects, rather than the minimization of the capacitance of PCB traces and bond pads as taught by Miller et al.

In Col. 8, lines 56-60 of Miller et al. it is stated that: "The present invention relates to interconnect systems for conveying I.O. signals between an IC and external circuits, and in particular to a method for merging the design of IC interconnect systems into the process of designing of the ICs themselves." By contrast, subject claims 1 and 4 model the IC in order to properly select the package traces.

In Col 18, lines 28-43, of Miller et al. it is stated that: "While the conventional approach to reducing the amount of signal distortion and attenuation caused by the interconnect system has been to minimize the inductance and capacitance of the interconnect systems, since it is not possible to completely eliminate interconnect system inductance, an unacceptable level of signal distortion and attenuation is inevitable when signal frequencies are sufficiently high. However as discussed above, further improvements in interconnect system frequency response can be had by actually increasing and appropriately arranging system inductance and capacitance. While lower values of interconnect system inductance and capacitance generally improve system frequency response, particular values of system inductance and capacitance that are higher than minimum attainable values can substantially improve various characteristic of system frequency response."

Thus, Miller et al. teaches away from the conventional approach of minimizing capacitance and inductance of the IC/interconnect system, and there is no mention or teaching by Miller et al. of selecting package traces to minimize package stub effects as taught in the present Specification and claimed in subject claims 1 and 4.

Since applicants do not believe that Miller et al. anticipates subject independent claims 1 and 4, applicants believe that no further response is required to the rejection of dependent claims 2 and 3, and 5 and 6, which depend therefrom, respectively.

In view of the discussion presented hereinabove, applicants believe that subject claims 1-6, as amended, are in condition for allowance, and such action by the Examiner at an early date is earnestly solicited.

Reexamination and reconsideration are respectfully requested.

Respectfully submitted,

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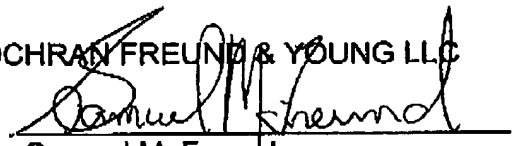
By: 

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